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AMENDMENTS TO THE CLAIMS

IN THE CLAIMS:

Please amend claims 17-20. Please add new claims 21-25. The claims are as follows:

17. (Currently Amended) A method of fabricating a semiconductor device comprising the steps of:

(a) providing a semiconductor wafer having a buried insulator layer;

(b) forming a fin on a said buried insulator layer of said semiconductor wafer;

(c) providing a first dielectric on said fin;

(d) depositing a first conductive material for a floating gate on said first dielectric;

(e) providing an insulator layer on said first conductive material;

(f) depositing a second layer of conductive material for a control gate on said insulator layer; and

(g) patterning said second layer of conductive material and said first conductive material.

18. (Currently Amended) The method of Claim 18 further comprising in step ~~(c)~~ (d) the step of spacer etching said first conductive material to form a spacer floating gate.

19. (Currently Amended) The method of claim 18 further comprising in step ~~(c)~~ (d) the step of spacer etching said first conductive material to form a double spacer floating gate.

20. (Currently Amended) The method of Claim 18 wherein step ~~(a)~~ (b) further comprises the step of forming a hard mask material on top of said fin to protect said fin where it extends beyond said second conductive material.

21. (New) The method of claim 17 wherein said fin has a sidewall, and further comprising forming a source region that includes a first portion of the sidewall and forming a drain region that includes a second portion of the sidewall.

22. (New) The method of claim 17 wherein the buried insulator layer is a buried oxide layer.

23. (New) The method of claim 22 wherein said buried insulator layer is formed on said semiconductor wafer by using thermal oxidation.

24. (New) The method of claim 17 wherein said fin is formed sufficiently thin as to provide full depletion when the device is in operation.

25. (New) The method of claim 17 wherein the semiconductor device is configured for horizontal current flow.